Reconfigurable Solutions For Adaptive Path Prediction

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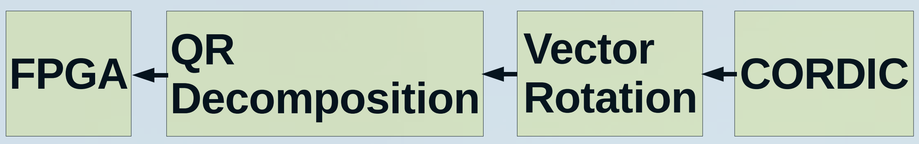
Theme: F
Project: F304-FIS

Introduction

- Following the project theme of **Intelligent Systems and Sensors**, used to increase the **safety** of modern vehicles
- Overall project: **Inertial Sensor Cluster for Adaptive Path Prediction**
- Dynamic model is a set of differential equations describing the maneuvering capabilities of the vehicle
  - **Kalman filter**. Computationally intensive: Use FPGA



- Many common mathematical operations are required in the course of computing a complex algorithm. To maximize overall efficiency, these operations themselves must be as efficient as possible: consider CORDIC

CORDIC (COordinate Rotation DIgital Computer)

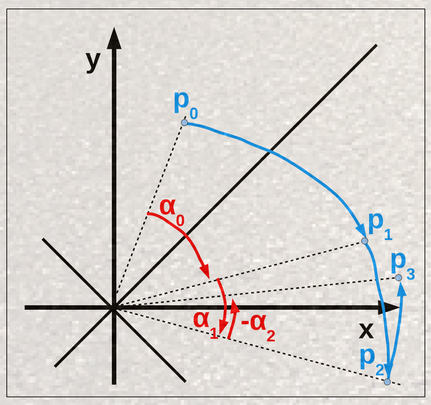
- CORDIC is a cheap method to compute many transcendental functions
  - Trigonometric and hyperbolic functions, as well as exponential functions, logarithms, multiplications, divisions, and square roots.
- **Advantages**
- Requires no hardware multiplier; only shift, addition and subtraction operations, and table lookup are used
- Therefore performs faster in most cases, (especially when no hardware multiplier is available)
- Minimizes number of gates required to implement supported functions, most useful for FPGA applications
- **Disadvantages**
- When hardware multiplier available can be slower than table lookup methods (eg in DSP microprocessor)

Method of Computation

- Using only bitshift and addition operations, (and LUT access) vectors can be rotated, due to rotation operation of:
- $x^{(i+1)} = x^{(i)} - y^{(i)}\tan\alpha^{(i)}$;
- $y^{(i+1)} = y^{(i)} + x^{(i)}\tan\alpha^{(i)}$;
- $z^{(i+1)} = z^{(i)} - \alpha^{(i)}$;
- Where $\tan\alpha^{(i)} = d_i \bullet 2^{-1}$, $d_i \in \{-1,1\}$

Example

- To compute the square root or magnitude of two numbers, a vector can be rotated to a point where y = 0, and x = magnitude of vector, as in the adjacent figure
- Conversion between cartesian and polar co-ordinates is possible.

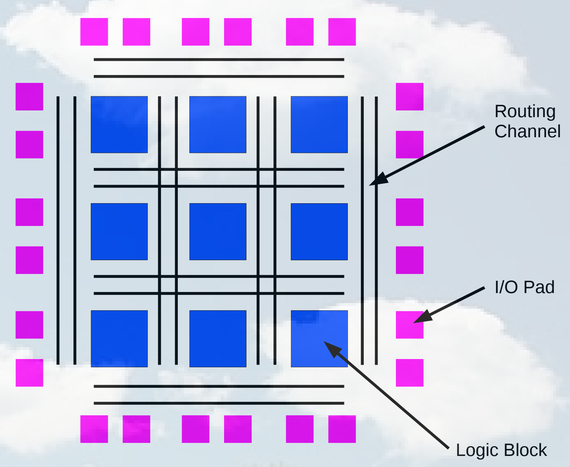


Precision

- CORDIC can compute to arbitrary precision, however, finite registers on processor limit precision of result
- Computation wise, at minimum, each additional bit of precision requires another iteration of processing

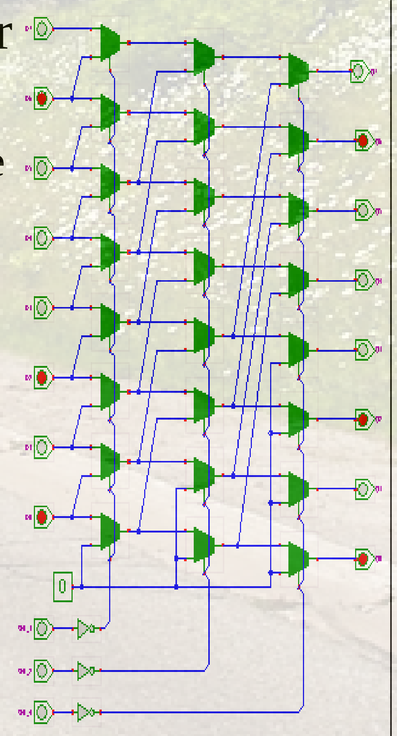
FPGA

- Field-programmable gate array is an integrated circuit that is configured after manufacturing, in "field"
- Contain programmable logic units which are "wired together" as in the following diagram
- Logic blocks can be configured to compute complex combinational functions or simple gates
- **Interconnects**
- Are reconfigurable
- Are slow
- Main FPGA bottle-neck
- Programmer must design to minimize interconnect usage



CORDIC on a FPGA

- **Consists of Barrel Shifter, adder, subtractor, and LUTs**
- **Barrel Shifter**
- Three Options: Rolled,Unrolled and Partially Rolled
- **Rolled**, Requires Barrel Shifter
- Separate modules exist on FPGA
- Less space but more interconnect use
- Slower operation; signal travels between modules: interconnect use
- Faster clock frequency
- Not necessarily faster overall operation
- **Unrolled,** No Barrel Shifter
- Combinational method
- Larger footprint
- Slower clock frequency
- Possibly faster overall computation
- **Partially Rolled**
- Combination of above two methods with more combinational parts than Rolled



Barrel Shifter

Applications

- Trigonometric and hyperbolic functions as well as exponential functions, logarithms, multiplications, divisions, and square roots.
- Linear algebra, (QR, SVD)
- **Kalman filter** for **Adaptive Path Prediction**